

Please amend the claims as follows:

Sub
B1
A1

1 1. (Amended) A processor for reading instructions from a memory
2 according to a program counter, and for executing the read instruction,
3 the program counter including a first program counter and a second
4 program counter,
5 the first program counter indicating a storage position of a processing
6 packet in the memory, the processing packet being made of an integer number of
7 bytes, the storage position being a position corresponding to a byte boundary,
8 the second program counter indicating a position of processing target
9 instruction in the processing packet regardless of whether the position corresponds
10 to a byte boundary, the processing target instruction being an operation to be
11 executed by the processor.

Sub C1
A2

1 11. (Amended) The processor of Claim 10, further including
2 an instruction buffer for temporarily storing instructions; and
3 instruction reading means for transferring instructions being made of an
4 integer number of bytes from the memory to the instruction buffer, in accordance
5 with available space in the instruction buffer but regardless of a size of a
6 processing packet.